ABSTRACT

A dynamic random access memory (DRAM) cell is described, including a semiconductor pillar on a substrate, a capacitor on a lower portion of a sidewall of the pillar, and a vertical transistor on an upper portion of the sidewall of the pillar. The capacitor includes a first plate in the lower portion of the sidewall of the pillar, a second plate as an upper electrode at the periphery of the first plate, a third plate at the periphery of the second plate electrically connected with the first plate to form a lower electrode, and a dielectric layer separating the second plate from the first and third plates. A DRAM array based on the DRAM cell and a method for fabricating the DRAM array are also described.